

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Om P. Agrawal; Hans W. Klein; Geoffrey R. Rickard; Harald J. Weller
Assignee: Lattice Semiconductor Corporation
Title: Clock Generator With Skew Control
Serial No.: 10/629,221 Filing Date: 07/29/2003
Examiner: Unassigned Group Art Unit: 2816
Docket No.: M-15206 US

Irvine, California
December 16, 2003

COMMISSIONER FOR PATENTS
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

UNDER 37 C.F.R. §1.97 AND § 1.98

Dear Sir:

Pursuant to 37 C.F.R. §1.97 and §1.98, Applicant calls the following documents (copies enclosed) to the attention of the Examiner. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom. Note that U.S. patent application no. 10/629,223, is being submitted for the Examiner to consider regarding double patenting.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made, or
3. an admission that the information cited herein is, or is considered to be material to patentability as defined in §1.56(b).

Applicant(s) believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 50-2257. Please deduct any additional fees from, or credit any overpayment to the above-noted Deposit Account.

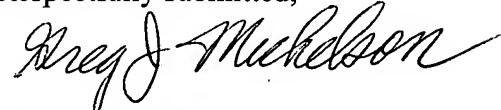
I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450, on December 16, 2003.



Eric Hoover

December 16, 2003

Respectfully submitted,



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U.S. Department of Commerce, Patent and Trademark Office		Atty Docket No.	Serial No.
		M-15206 US	10/629,221
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		Applicant(s)	
		Om P. Agrawal et al.	
		Filing Date	Group
		07/29/2003	2816



U.S. Patent Documents

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
AA						
AB						
AC						
AD						
AF						
AF						
AG						
AH						
AI						
AJ						
AK						

Foreign Patent Documents

		Document	Date	Country	Class	Subclass	Translation
	AF						
	AM						
	AN						
	AO						
	AF						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AQ	U.S. Patent Application No. 10/629,223 entitled "Clock Generator" filed on July 29, 2003	
AR	3.3V Programmable Skew PLL Clock Driver Turboclock, IDT5V991A, Commercial and Industrial Temperature Ranges, September 2001	
AS	One-PLL General Purpose Flash-Programmable Clock Generator, CY22050, Cypress Semiconductor Corporation, San Jose, CA, Revised December 14, 2002	

Examiner	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
Foreign Patent Documents							
		Document	Date	Country	Class	Subclass	Translation
	AL						Yes
	AM						No
	AN						
	AO						
	AP						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AQ	ICS541, PLL Clock Divider, Revision 021303, Integrated Circuit Systems, Inc.					
	AR	User Programmable Laser Engine Pixel Clock Generator, ICS1574B, 08/31/2000					
	AS	EEPROM Programmable 3-PLL Clock Generator IC, FS6370-01, AMI Semiconductor					
Examiner		Date Considered					
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